Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1-38. (canceled)

39. (previously presented) An apparatus for processing packets, comprising:

a first input queue configured to receive a stream of incoming packets and to output beginning portions of packets as the beginning portions are received without waiting for the respective packets to be received in their entirety;

a first in-line packet processor for receiving the beginning portions from the first input queue, each beginning portion including first header information, and for detecting the existence of an error in the first header information of each beginning portion; and

a first memory for storing packets received at the first input queue and for which the first in-line packet processor did not detect an error in the corresponding first header information.

40. (previously presented) The apparatus of claim 39, wherein the errors that the first in-line packet processor detects include at least one of unrecognized header format, failure to match a header pattern, incorrect checksum, or incorrect packet length.

41. (previously presented) The apparatus of claim 39, wherein the first in-line packet processor generates a signal to drop a packet before the packet is stored in the first memory and for which it detects an error in the corresponding first header information.

42. (previously presented) The apparatus of claim 39, wherein each beginning portion includes second header information, where the first header information comprises link layer header information and the second header information comprises network layer header information.

43. (previously presented) The apparatus of claim 39, wherein each beginning portion includes second header information, and

wherein the first in-line packet processor further detects the existence of an error in the second header information.

44. (previously presented) The apparatus of claim 39, wherein the first memory stores packets received at the first input queue and for which the first in-line packet processor did not detect an error in the corresponding first header information or in second header information contained in the packet.

45. (previously presented) The apparatus of claim 39, further comprising:

a second input queue configured to receive a stream of incoming packets and to output beginning portions of packets as the beginning portions are received without waiting for the respective packets to be received in their entirety; and

a second in-line packet processor for receiving the beginning portions from the second input queue, each beginning portion including first header information, and for detecting the existence of an error in the first header information of each beginning portion.

46. (previously presented) The apparatus of claim 45, wherein the first memory further stores packets received at the second input queue and for which the second in-line packet processor did not detect an error in the corresponding first header information.

47. (previously presented) The apparatus of claim 45 further comprising a second memory for storing packets received at the second input queue and for which the second in-line packet processor did not detect an error in the corresponding first header information.

48. (previously presented) The apparatus of claim 39, wherein the first memory stores packets without the respective first header information corresponding to the packets that are received at the first input queue and for which the first in-line packet processor did not detect an error in the corresponding first header information.

49. (previously presented) A device for processing packets, comprising:

an input queue for receiving a stream of packets and for outputting beginning portions of packets as the beginning portions are received without waiting for the respective packets to be received in their entirety;

a header processor configured to receive the beginning portions from the input queue, each beginning portion including first header information, for detecting the existence of an error in the first header information included in each beginning portion,

wherein upon detecting the existence of an error in a first header information, the header processor generates an error signal indicating that the corresponding packet contains an error; and

a buffer manager for causing each packet received at the input queue to be stored in memory if the buffer manager does not receive an error signal corresponding to the packet from the header processor.

50. (canceled)

51. (previously presented) The device of claim 49, wherein the beginning portions contain second header information for respective packets, and

wherein the header processor detects the existence of an error in the first header information or the second header information and generates an error signal for a packet if

the header processor detects an error in the corresponding first header information or second header information of the packet.

52. (previously presented) The device of claim 51, wherein the first header information comprises link layer header information and the second header information comprises network layer header information.

53. (previously presented) A device for packet processing, comprising:

an input queue for sequentially receiving portions of a packet, a first portion including a first packet header, and for outputting the first portion before the remaining portions are received;

a header processor, coupled to the input queue, configured to process the first packet header included in the first portion prior to transferring any portions of the packet into a packet memory; and

a buffer manager, coupled to the input queue and the header processor, configured to cause the portions of the packet received at the input queue to be stored in the packet memory if no signal is received from the header processor to drop the packet.

54. (previously presented) The device of claim 53, wherein the portions of the packet stored in the packet memory by the buffer manger do not include the first packet header.

55. (previously presented) The device of claim 53, wherein the first portion further includes a second packet header for the packet, and

wherein the header processor further processes the second packet header.

56. (previously presented) The device of claim 55, wherein the first packet header comprises a layer 2 header and the second packet header comprises a layer 3 header.

57. (previously presented) The device of claim 53, wherein the processing performed by the header processor includes detecting the existence of any errors in the first packet header.

58. (previously presented) The device of claim 53, wherein the processing performed by the header processor includes comparing the first packet header to at least one prestored packet format.

59. (previously presented) A device for packet processing, comprising:

an input queue for sequentially receiving portions of a packet, a first portion including a first packet header for the packet, and for outputting the first portion before the remaining portions are received;

a header processor, coupled to the input queue, configured to process the first packet header included in the first portion prior to transferring any portions of the packet into a packet memory; and

a buffer manager, coupled to the input queue and the header processor, configured to cause the portions of the packet received at the input queue to be stored in the packet memory after receiving a signal from the header processor indicating acceptance of the packet.

60. (previously presented) The device of claim 59, wherein the portions of the packet stored in the packet memory by the buffer manger do not include the first packet header.

61. (previously presented) The device of claim 59, wherein the first portion further includes a second packet header for the packet, and

wherein the header processor further processes the second packet header.

62. (previously presented) The device of claim 61, wherein the first packet header comprises a layer 2 header and the second packet header comprises a layer 3 header.

63. (previously presented) The device of claim 59, wherein the processing performed by the header processor includes detecting the existence of any errors in the first packet header.

64. (previously presented) The device of claim 59, wherein the processing performed by the header processor includes comparing the first packet header to at least one prestored packet format.

65. (currently amended) A method of processing a packet, comprising:

receiving portions of a packet in a stream at a first input queue;

forming a beginning portion of the packet as the portions are received without waiting for the entire packet to be received, the beginning portion containing first header information;

outputting the beginning portion to a first in-line packet processor;

while the remaining portions of the packet are being received at the first input queue, detecting the existence of an error in the beginning portion at the first in-line packet processor; and

dropping the packet upon existence of an error in the packet.

66. (previously presented) The method of claim 65, wherein the dropping comprises preventing the packet from being stored in memory.

67. (previously presented) The method of claim 65, wherein the detecting comprises determining whether the first header information matches a prestored header pattern.

68. (previously presented) The method of claim 65, wherein the detecting comprises determining whether a header checksum contained in the first header information is correct.

69. (previously presented) The method of claim 65, wherein the first header information comprises link layer header information.

70. (previously presented) The method of claim 65, wherein the first header information comprises network layer header information.

71. (previously presented) The method of claim 65, further comprising:

storing the packet in memory if the existence of an error is not detected.

72. (previously presented) The apparatus of claim 39, further comprising:

a plurality of output line interfaces configured to output respective streams of outgoing packets;

a lookup processor for determining an output line interface for each packet stored in the first memory based on second header information contained in the packet; and

a controller for facilitating transmission of packets from the first memory to the respective output line interfaces determined by the lookup processor.